

CLAIMS

1. A circuit for reading a memory cell, the circuit comprising:
 - a read node operable to receive a read current from the memory cell;
 - a first current source operable to provide a first bias current to the read node;
 - a first transistor having a control terminal and a first conduction terminal coupled to the read node;
 - a reference node;
 - a reference generator operable to provide a reference current to the reference node;
 - a second current source operable to provide a second bias current to the reference node; and
 - a second transistor having a control terminal coupled to the read node and having a first conduction terminal coupled to the reference node.
2. The circuit of claim 1, further comprising:
 - first and second supply nodes;
 - wherein the first and second current sources are coupled to the first supply node; and
 - wherein the first and second transistors each have a respective second conduction terminal coupled to the second supply node.
3. The circuit of claim 1 wherein the first bias current equals the second bias current.
4. The circuit of claim 1 wherein:
 - the first and second current sources each comprise a respective PMOS transistor; and
 - the first and second transistors each comprise a respective NMOS transistor.

5. The circuit of claim 1, further comprising:
 - a third transistor having a control terminal and a conduction terminal coupled to the read node; and
 - a fourth transistor having a control terminal and a conduction terminal coupled to the reference node.
6. The circuit of claim 1, further comprising:
 - a bias generator operable to generate a bias voltage; and
 - wherein the first and second current sources are operable to generate the first and second bias currents in response to the bias voltage.
7. The circuit of claim 1, further comprising a comparator having first and second input terminals respectively coupled to the read and reference nodes.
8. The circuit of claim 1, further comprising a precharger coupled to the read node.
9. A method for reading a memory cell, the method comprising:
 - sourcing a first bias current to a read node;
 - sinking a read current from the read node;
 - sinking from the read node a first difference current that is inversely proportional to the read current;
 - sourcing a second bias current to a reference node;
 - sinking a reference current from the read node; and
 - sinking from the reference node a second difference current that is inversely proportional to the read current.
10. The method of claim 9 wherein the first bias current equals the second bias current.

11. The method of claim 9, further comprising comparing a voltage on the read node to a voltage on the reference node to determine a data value stored in the memory cell.

12. The method of claim 9, further comprising sinking from the read node a third difference current that is inversely proportional to the read current.

13. The method of claim 9, further comprising sinking from the reference node a third difference current that is proportional to the read current.

14. Sensing circuitry for reading and verifying the contents of electrically programmable and erasable non-volatile memory cells, which circuitry comprises a sense amplifier having a first sensing circuit portion connected to a cell to be read and provided with an output terminal for connection to a first input terminal of a comparator, and having a second reference circuit portion connected to a reference current generator and provided with an output terminal for connection to a second input terminal of said comparator, characterized in that said first and said second circuit portions comprise a series of first and second transistors, respectively, being connected between a first voltage reference and a second voltage reference and having respective points of interconnection taken to said output terminals of said first and second circuit portions.

15. Sensing circuitry according to claim 14, characterized in that said second transistor in said second circuit portion comprises a parallel of third and fourth transistors, the control terminal of said fourth transistor being connected to said output terminal of said first circuit portion.

16. Sensing circuitry according to claim 14, characterized in that it comprises a bias and precharge block connected between a first voltage reference and a second voltage reference, as well as connected to control terminals of said first transistors in

said first and second circuit portions and to the control terminal of said second transistor in said first circuit portion.

17. Sensing circuitry according to claim 14, characterized in that said first transistors in said first and second circuit portions are PMOS transistors, and said second transistors in said first and second circuit portions are NMOS transistors.

18. Sensing circuitry according to claim 14, characterized in that said second transistor in said first circuit portion comprises a pair of transistors, being connected in parallel with each other in a diode configuration and having control terminals connected to said output terminal of said first circuit portion.

19. Sensing circuitry according to claim 16, characterized in that said first transistors in said first and second circuit portions have interconnected control terminals.

20. Sensing circuitry according to claim 19, characterized in that said bias block has a first leg and a second leg, with said first leg comprising a cascade of a first transistor in a diode configuration and a second transistor, and said second leg comprising a cascade of a first transistor and a second transistor, the control terminal of said second transistor in said first leg being connected to a shared node of said first transistor and second transistor in said second leg.

21. Sensing circuitry according to claim 20, characterized in that said first transistor in said first leg forms a current mirror configuration with the first transistors in said first and second circuit portions.

22. Sensing circuitry according to claim 20, characterized in that said first transistor in said first leg and said first transistor in said second leg form a current mirror.

23. Sensing circuitry according to claim 20, characterized in that said second transistor in said second leg is a cascade of third and fourth transistors, said second leg further comprising a fifth transistor connected between a shared node of said third and fourth transistors and said second voltage reference, said fifth transistor having a control terminal connected to a control terminal of said second transistor in said first circuit portion.

24. Sensing circuitry according to claim 14, characterized in that said comparator includes a current mirror formed of first and second transistors, with said first transistor being a diode configuration.

25. Sensing circuitry according to claim 24, characterized in that said first transistor of said comparator is connected in series with a third transistor, and that said second transistor of said comparator is connected in series with a fourth transistor, said third transistor having a control terminal connected to the node, and said transistor having a control terminal connected to said node).

26. Sensing circuitry according to claim 25, characterized in that said third transistor and fourth transistor of said comparator, and said second transistor in said first circuit portion and said second transistor in said second circuit portion, are all the same size.

27. Sensing circuitry according to claim 16, characterized in that it comprises an auxiliary precharge circuit connected between said first and said second voltage reference, said auxiliary precharge circuit including a current mirror formed of first and second transistors, with said first transistor being a diode a configuration, said auxiliary precharge circuit further including a third transistor connected in series with said first transistor, the second transistor being connected to said first node.

28. Sensing circuitry according to claim 27, characterized in that said auxiliary precharge circuit also has a leg comprising a first transistor connected in cascade with a second transistor, the latter in a diode configuration, and comprising a third transistor

connected in parallel with said transistor, a control terminal of said third transistor and a control terminal of said second transistor of said mirror in said auxiliary precharge circuit being connected together.